

IN THE CLAIMS:

Please cancel claims 1-3 in their entirety without prejudice nor disclaimer of the subject matter set forth therein, amend claims 4 and 5 and add new claim 9 as follows.

1 – 3. (Canceled)

4. (Currently Amended) An interface circuit provided for each of a first device set as a master side and a second device set as a slave side, for performing a serial data transmission between the first and second devices on the basis of a control signal which is output from the master side, comprising:

an oscillation circuit which generates a clock signal for data transmission ~~upon receiving an operation enable signal;~~

~~a transmission function portion which performs a serial data transmission with the other device upon receiving the clock signal;~~

a detection portion which monitors the control signal to output a detection signal when there is a change in the ~~detection control~~ control signal; and

a process control portion which ~~performs control of the~~ generates a operation-enable clock-control signal on the basis of which alternately changes between clock-enable and clock-disable states each time the detection signal is supplied thereto, and stops the operation of the oscillation circuit while the clock-control signal is in the disable-state; and

a transmission function portion which performs a serial data transmission with the other device on the basis of the clock signal.

5. (Currently Amended) The interface circuit according to claim 4, wherein the detection portion comprises:

a first flip-flop which is set at either one of the timings of a rise and a fall of the control signal;

a second flip-flop which holds an output signal of the first flip-flop;

a delay gate which delays an output signal of the second flip-flop by a predetermined time period; and

~~a comparator gate circuit which compares~~ detects the change of the control

signal on the basis of the output signal of the delay gate with and the output signal of the first flip-flop to detect a change therein of the control signal.

6. (Original) The interface circuit according to claim 4, wherein the detection portion comprises:

a register which holds an expected value supplied from the process control portion in accordance with the state of the control signal; and

a comparator circuit which compares the expected value held in the register with the control signal to output the detection signal on the basis of the comparison result;

wherein the process control portion is configured so as to perform control of the operation-enable signal in response to the detection signal, while re-writing the register value of the detection portion with the expected value for the next control signal in response to the detection signal.

7. (Original) The interface circuit according to claim 4, wherein the detection portion comprises:

a register which holds an expected value supplied from the process control portion in accordance with the state of the control signal in synchronization with the clock signal; and

a comparator circuit which compares the expected value held in the register with the control signal to output the detection signal on the basis of the comparison result;

wherein the process control portion is configured so as to perform control of the operation-enable signal in response to the detection signal, while supplying the expected value for the next control signal to the register of the detection portion in response to the detection signal.

8. (Original) The interface circuit according to claim 6, wherein the detection portion comprises:

a noise removal circuit which removes noise components having short pulse widths contained in the control signal.

9. (New) The interface circuit according to claim 7, wherein the detection portion includes a noise removal circuit for removing a noise that is superimposed on the control signal.